DERWENT-ACC-NO: 2000-045807

DERWENT-WEEK: 200222

TITLE: Packaging structure of semiconductor device - has semiconductor chip mounted on island portion connected to lead portion through electrode on insulated substrate and is surrounded by resin layer

PATENT-ASSIGNEE: SANYO ELECTRIC CO LTD[SAOL]

PRIORITY-DATA: 1998JP-0106519 (April 16, 1998)

PATENT-FAMILY:

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INT-CL (IPC): H01L023/12, H01L023/48

ABSTRACTED-PUB-NO: JP 11307673A

BASIC-ABSTRACT:

NOVELTY - Island portion (13) and lead portion (14) are formed on insulated substrate (11a) which is attached to bipolar electrodes

(19,20) fixed over
other insulated substrate (11b). Semiconductor chip (12) is mounted on island
portion and is electrically connected to lead portion through inclined external
electrode. Notch portion provides electrically conductive pattern on which
electrode is placed. DETAILED DESCRIPTION - Resin layer provided over one
insulated layer coats semiconductor chip, island and lead portion, surface
cutting resin layer and insulated layers simultaneously, on peripheral end. An
INDEPENDENT CLAIM is also included for manufacturing method of semiconductor
device.

USE - In semiconductor device.

ADVANTAGE - High density package of semiconductor is obtained as lead terminal
is not protruding the surface. Gold plating layer does not expose resin layer
and hence peeling of resin layer is avoided during any accident. DESCRIPTION
OF DRAWING(S) - The figure shows the top view of semiconductor device.
(11a,11b) Insulated substrates; (12) Semiconductor chip;
(13) Island portion;
(14) Lead portion; (19,20) Bipolar electrodes.

CHOSEN-DRAWING: Dwg.1/7

TITLE-TERMS: PACKAGE STRUCTURE SEMICONDUCTOR DEVICE SEMICONDUCTOR CHIP MOUNT
ISLAND PORTION CONNECT LEAD PORTION THROUGH ELECTRODE INSULATE
SUBSTRATE SURROUND RESIN LAYER

DERWENT-CLASS: U11

EPI-CODES: U11-D01A3; U11-E01A;

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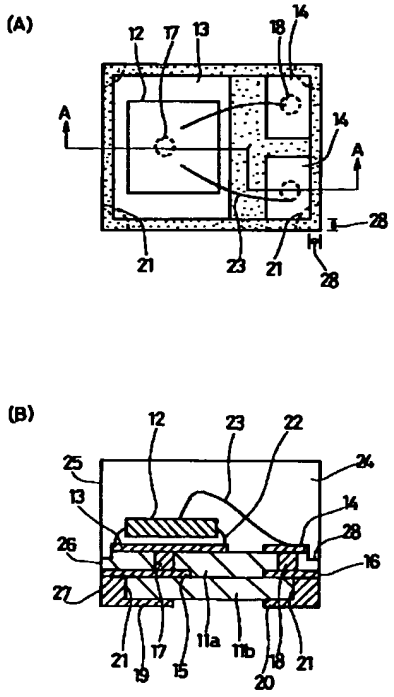
(54)【発明の名称】　半導体装置とその製造方法

(57)【要約】

【課題】　実装面積を縮小した小型のパッケージを得ると共に、実装時の半田の吸着による事故を回避した、半導体装置を提供する。

【解決手段】　第１の絶縁基板１１ａの表面にアイランド部１３とリード部１４を形成し、スルーホール１７、１８と切り欠き部２１を介して外部電極１９、２０と電気的に接続する。アイランド部１３に半導体チップ１２を搭載し、リード部１４とワイヤボンドする。半導体チップ１２上を樹脂層２４で被覆し、ダイシングすることで第１と第２の絶縁基板１１ａ、１１ｂの外周端面２６、２７と樹脂層２４の外周端面２５とを連続した同一水平面とする。外周端面２６付近からアイランド部１２とリード部１３の金メッキ層を後退させる。



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【特許請求の範囲】

【請求項1】　貼着して支持基板を形成する第1と第2の絶縁基板と、

前記第1の絶縁基板の表面に導電体パターンによって形成したアイランド部、及びリード部と、

前記アイランド部に搭載した半導体チップと、

前記半導体チップの電極と前記リード部とを電気的に接続する手段と、

前記第1の絶縁基板の上に設けられて前記半導体チップ及び前記アイランド部と前記リード部とを被覆する樹脂層と、

前記第1の絶縁基板と第2の絶縁基板の間に設けた中間電極と、

前記第2の絶縁基板の裏面側に形成され、前記アイランド部またはリード部と前記中間電極を介して電気的に接続された外部電極と、

前記第2の絶縁基板の角部に設けられ、その表面に前記外部電極と連続する導電パターンが設けられた切り欠き部と、

前記第1と第2の絶縁基板の外周端面と、

前記樹脂層の外周端面とを具備し、

前記第1と第2の絶縁基板の外周端面と前記樹脂層の外周端面とがほぼ一致し、

前記アイランド部と前記リード部の導電体パターンが前記外周端面より内側に位置し、

前記外周端面付近では前記第1の絶縁基板の素材と前記樹脂層とが密着していることを特徴とする半導体装置。

【請求項2】　前記外周端面が前記樹脂層と前記第1と第2の絶縁基板とを同時に切断した切断面で構成されていることを特徴とする請求項1記載の半導体装置。

【請求項3】　前記第1の絶縁基板の外周端面付近に溝を設けたことを特徴とする請求項1記載の半導体装置。

【請求項4】　その表面に複数個の半導体素子を形成するための導電体パターンを形成した第1の絶縁基板と、外部接続用の外部電極を形成した第2の絶縁基板とを、前記導電体パターンと前記外部電極とが電気的に接続されるように貼着し、大判の基板を構成する工程と、

前記導電体パターンを前記第1の絶縁基板の端から後退させる工程と、

前記導電体パターンに半導体チップを固着する工程と、

前記半導体チップを被覆するように前記第1の絶縁基板の上部を樹脂層で被覆する工程と、

前記半導体チップの周囲で、前記樹脂層と前記第1と第2の絶縁基板とを切断して前記半導体素子を個々に分離する工程と、を具備することを特徴とする半導体装置の製造方法。

【請求項5】前記導電体パターンと共に前記第1の絶縁基板の表面をダイシングすることにより、前記導電体パターンをパッケージ外周予定部位より後退させたことを特徴とする請求項4記載の半導体装置の製造方法。

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【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は半導体装置に関し、特にパッケージ外形を縮小し、実装面積を低減できる半導体装置に関する。

【0002】

【従来の技術】半導体装置の製造におけるパッケージングの技術には、金型と樹脂注入によるトランスファーモールドが多用されている。このトランスファーモールド技術にはリードフレームが用いられており、1本のリードフレームで複数の半導体装置を同時に製造することになる。

【0003】図6（A）はトランスファーモールド工程を示す図である。ダイボンド、ワイヤボンドにより半導体チップ1をリードフレーム2に固着し、上下金型3A、3Bで形成したキャビティ4の内部にリードフレーム2を設置し、キャビティ4内にエポキシ樹脂を注入することにより、半導体チップ1の封止が行われる。このようなトランスファーモールド工程の後、リードフレーム2を各半導体チップ1毎に切断して、個別の半導体装置が製造される。

【0004】図6（B）は、トランスファーモールドによって製造した半導体装置を示す図である。トランジスタ等の素子が形成された半導体チップ1がアイランド5上に半田等のろう材6によって固着実装され、半導体チップ1の電極パッドとリード7とがワイヤ8で接続され、半導体チップ1の周辺部分が上記キャビティの形状に合致した樹脂9で被覆され、樹脂9の外部にリード7の先端部分が導出されたものである。

【0005】

【発明が解決しようとする課題】従来のリードフレームとトランスファーモールドを用いたパッケージでは、外部接続用のリード端子を樹脂から突出させるので、リード端子の先端部までの距離を実装面積として考慮しなくてはならず、樹脂の外形寸法より実装面積の方が遥かに大きくなるという欠点がある。

【0006】そのため、外部接続リードに半田バンプなどを用いることで外形寸法と実装面積とをほぼ等しくするような手法や、実装基板上にベアチップを直接ダイボンドする方法等が提案されている。

【0007】このような命題に対し、本願出願人は、絶縁基板とダイシング技術を用いることにより、実装面積を大幅に低減した半導体装置を特願平9－262160号に提案した。

【0008】斯かる装置は、図7を参照して、第1の絶縁基板51に導電パターンによりアイランド部52とリード部53を設け、半導体チップ54をダイボンド、ワイヤボンドし、第2の絶縁基板55の裏面に外部電極56を設け、更に第2の絶縁基板55の4隅に導電メッキを施した切り欠き57を設けて外部電極56と接続し、

該外部電極５６とアイランド部５２及びリード部５３とを中間の導電体パターン５８とスルーホール５９とにより電気的に接続したものである。パッケージの外形寸法は金型のキャビティで決めるのではなく、半導体チップ５４の周囲で樹脂６０と共にダイシングで切断することにより形成している。これを実装するときは、切り欠き５７内面に露出する導電メッキ層と共に第２の絶縁基板５５裏面に形成した外部電極５６を電極として、実装基板に半田で接着するものである。この構造は、リード端子が突出しないので、実装面積を大幅に低減する事ができる。尚、図７（Ｂ）は図７（Ａ）のＢＢ線断面図である。

【０００９】しかしながら、斯かる構造では樹脂６０と第１の絶縁基板５１の境界部分にアイランド部５２とリード部５３の導電パターンの端面が露出した構造となる。導電パターンに用いる金（Au）は半田との塗れ性が極めて高いため、実装用の半田が前記導電パターンの端面に達すると半田を吸着してしまい、第１の絶縁基板５１と樹脂６０との境界に半田が侵入して剥がれ不良を生じることが明らかになった。

【００１０】

【課題を解決するための手段】本発明は上述した各事情に鑑みて成されたものであり、第１に、複数の絶縁基板を貼着して形成した基板上に複数の半導体チップを搭載し、半導体チップを樹脂層で封止し、半導体チップを囲むように樹脂と絶縁基板とをダイシング・切断することにより、装置の外形寸法及び実装面積を大幅に低減できる半導体装置を提供するものである。

【００１１】第２に、第１の絶縁基板の表面に形成した導電体パターンを、第１の絶縁基板の外周端面から内側に後退させることにより、導電体パターンが外周端面に露出することを防止し、もって実装時のはんだが樹脂層と第１の絶縁基板との間に吸着される事故を防止するものである。

【００１２】

【発明の実施の形態】以下に本発明の実施の形態を詳細に説明する。

【００１３】図１は本発明の半導体装置を示す（Ａ）平面図、（Ｂ）ＡＡ線断面図、図２（Ａ）は本発明の半導体装置を示す斜視図である。この半導体装置は、板厚が各々１５０～２５０μのセラミックやガラスエポキシ等からなる第１と第２の絶縁基板１１ａ、１１ｂと、第１の絶縁基板１１の上に搭載され、トランジスタ素子などを形成した半導体チップ１２とを有する。

【００１４】第１の絶縁基板１１ａの表面には、金メッキ層によってアイランド部１３とリード部１４とが形成されており、第１の絶縁基板１１ａの裏面にも金メッキ層により中間電極１５、１６が形成されている。中間電極１５、１６は、アイランド部１３、リード部１４のパターンと同等のパターンを有している。アイランド部１３とリード部１４の第１の絶縁基板１１ａにはスルーホール１７、１８が設けられており、該スルーホール１７、１８の内部がタングステン、Ａｇ－Ｐｄ等の導電材料によって埋設され、これによってアイランド部１３と中間電極１５、及びリード部１４と中間電極１６とが各々電気的に接続されている。

【００１５】第２の絶縁基板１１ｂの裏面には導電パターンにより外部電極１９、２０が形成されており、この外部電極１９、２０は第２の絶縁基板１１ｂの終端付近にまで延在している。第２の絶縁基板１１ｂの４隅には、円筒形の４分の１に相当する切り欠き部２１が形成されており、該切り欠き部２１の内周面にも導電パターンが形成されて、外部電極１９、２０と中間電極１５、１６とが電気的に接続される。結果、トランジスタのベース・コレクタ・エミッタに各々相当する外部電極１９、２０が形成される。

【００１６】そして、半導体チップ１２はアイランド部１３に銀ペーストや金シリコン共晶等の接着剤２２によって固着されており、半導体チップ１２表面に形成したボンディングパッドとリード部１４とが、ワイヤ２３でワイヤボンディングされている。これらの半導体チップ１２とワイヤ２３を被覆するように、第１の絶縁基板１１ａの上にエポキシ系の樹脂層２４を形成してこれを封止し、略直方体のパッケージを形成している。

【００１７】パッケージの外形は、上面が樹脂層２４により、下面が第２の絶縁基板１１ｂの裏面により、そして４つの側面が樹脂層２４と第１と第２の絶縁基板１１ａ、１１ｂの外周端面２５、２６、２７によって各々構成される。樹脂層２４の外周端面２５と、第１と第２の絶縁基板１１ａ、１１ｂの外周端面２６、２７とは連続する同一水平面を成している。

【００１８】そして、第１の絶縁基板１１ａの表面に形成したアイランド部１３とリード部１４の金メッキ層は、第１の絶縁基板１１ａの外周端面２６には達せず、第１の絶縁基板１１ａの全周にわたって、その端部から３０～７０μの距離だけ後退されている。後退された箇所には、第１の絶縁基板１１ａの外周端面２６に沿って半導体チップ１２の周囲を囲むように幅が３０～７０μ、深さ１００μ程度の溝２８が形成されている。

【００１９】図２（Ｂ）は、斯かる装置を実装した状態を示す断面図である。実装基板２９上に形成された回路網形成用のプリント配線３０に、装置の外部電極１９、２０を位置あわせして、半田により装置が固着される。半田は表面張力によって端部に盛り上がって半田フィレット３１を形成する。

【００２０】本発明の半導体装置であれば、切り欠き部２１の内面が金メッキ層等の導電パターンで被覆されているので、半田フィレット３１を大きく盛り上げることができる。このとき、アイランド部１３とリード部１４を後退させたことにより、樹脂層２４と第１の絶縁基板

１１ａの境界にこれらの金メッキ層が露出しないので、半田フィレット３１の半田を吸収することもない。そのため、樹脂層２４が剥離する事故を回避できる。また、溝２８を設けたことにより、第1の絶縁基板１１ａと樹脂層２４との密着面積が増大するので、両者の接着強度を増大できる。

【００２１】以上に説明した半導体装置は、以下の方法によって得ることができる。

【００２２】第1工程：図3（Ａ）参照

まずは装置複数個分に相当する大判の基板３２を準備する。この基板３２は、第1と第2の絶縁基板１１ａ、１１ｂを貼着したものである。第1の絶縁基板１１ａの表面には金メッキ層によりアイランド１３とリード部１４に対応するパターンが櫛歯状の連続パターンで描画されている。第2の絶縁基板１１ｂの裏面にも同様の連続パターンで外部電極１９、２０に対応する金メッキ層が形成される。アイランド１３とリード部１４の第1の絶縁基板１１ａには外部電極１９、２０と電気的接続を取るためのスルーホール１７、１８が設けられている。この段階では、アイランド部１３とリード部１４とは分離していない連続したパターンである。

【００２３】同図において、ダイシングライン３３で囲まれた領域が1つの半導体装置として後に切り出されることになる。そして、ダイシングライン３３の交差する箇所の第2の絶縁基板１１ｂには、切り欠き２１に相当するスルーホール３４が設けられている。

【００２４】斯かる状態の基板３２にに対して、多数の半導体チップ１２をダイボンドし、チップ上に形成したボンディングパッドとリード部１４とをボンディングワイヤ２３で接続する。

【００２５】第2工程：図3（Ｂ）

ダイシングライン３３を中心線として、これに沿うよう幅５０～８０μ、深さ約１００μの溝２８を形成する。溝２８はダイシングブレードを用いて金メッキ層と共に第1の絶縁基板１１ａ表面をダイシングすることによって形成する。これにより、溝２８を形成すると同時にアイランド部１３とリード部１４をダイシングライン３３から後退させることができる。

【００２６】第3工程：図4（Ａ）

第1の絶縁基板１１ａの上にポッティングなどの手法により樹脂層２４を形成する。樹脂層２４は半導体チップ１２を個別に被覆するものではなく、複数の半導体チップ１２を連続した樹脂で一括して被覆する。例えば一枚の基板３２に５０個の半導体チップ１２を搭載した場合は、５０個全てのチップを一括して被覆する。

【００２７】第4工程：図4（Ｂ）

ダイシングブレード３５により、ダイシングライン３３に沿って樹脂層２４と第1と第2の絶縁基板１１ａ、１１ｂを同時に切断し、個々の半導体装置に分離する。この工程では溝２８の幅よりも板厚が狭いダイシングブレードを用いており、これによって第1の絶縁基板１１ａの外周端面２６に溝２８を残し、アイランド部１３とリード部１４との金メッキ層が樹脂層２４の外周端面２５に露出しない構造を得ている。また、ダイシングライン３３の交差部分に設けたスルーホール３４はダイシングにより4分割されて切り欠き部２１を形成する。更に、ダイシングによってパッケージの4つの側面を構成することにより、それらの切断面（外周端面２５、２６、２７）が同一平面で構成される。

【００２８】以上の方法によって製造された半導体装置は、以下のメリットを有する。

【００２９】多数個の素子をまとめて樹脂でパッケージングするので、個々にパッケージングする場合に比べて、無駄にする樹脂材料を少なくでき。材料費の低減につながる。

【００３０】モールド金型とリードフレームとの位置合わせ精度がプラス・マイナス５０μ程度であるのに対して、ダイシング装置の位置あわせ精度はプラス・マイナス１０μ程度と精度が高い。従って樹脂外形をダイシングで形成すれば、アイランド部１３から樹脂２１の切断面までの肉厚を薄くして、より外形寸法の小さなパッケージを得ることができるほか、同じ外形寸法で比較すればアイランド部１３の面積を増大して、搭載可能な半導体チップ１２を大型化できる。

【００３１】尚、ダイシングで溝２８を形成する手段に代えて、アイランド部１３とリード部１４のパターンを形成する際に、あらかじめダイシングライン２６から後退させたパターンで形成することでも同様の構造を得ることができる。

【００３２】更に図5に示したように、溝２８の形成と同時的にアイランド部１３とリード部１４との間の空白部分にも溝２８ａを形成することにより、樹脂との密着強度を更に向上することも可能である。

【００３３】本実施形態では、半導体チップ１２にトランジスタを形成したが、縦型或いは比較的発熱量の少ない横型のデバイスであればこれに限らず、例えば、パワーMOSFET、IGBT、HBT等のデバイスを形成した半導体チップであっても、本発明に応用ができることは説明するまでもない。

【００３４】

【発明の効果】以上に説明したように、本発明によれば、リードフレームを用いた半導体装置よりも更に小型化できるパッケージ構造を提供できる利点を有する。このとき、リード端子が突出しない構造であるので、実装したときの占有面積を低減し、高密度実装を実現できる。

【００３５】更に、切り欠き部２１によって半田フィレット３１が容易に盛り上がる構造にできる。このとき、第1の絶縁基板１１ａと樹脂層２４との境界部分に金メッキ層が露出しない構成としたので、実装時の半田が境

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界部分に接触・吸い込まれて樹脂層２４が剥離する事故を回避することができる。

【００３６】加えて、第１の絶縁基板１１ａの外周部分に溝２８を形成することにより、第１の絶縁基板１１ａと樹脂層２４との密着力を増大できる他、溝２８をダイシングで形成することにより、金メッキ層の後退と溝２８の形成を同時的に実施することができる。く寄与することができる。

【図面の簡単な説明】

【図１】本発明の半導体装置を示す（Ａ）平面図、（Ｂ）断面図である。

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【図２】本発明の半導体装置を示す（Ａ）斜視図、（Ｂ）断面図である。

【図３】本発明の半導体装置の製造方法を説明する図である。

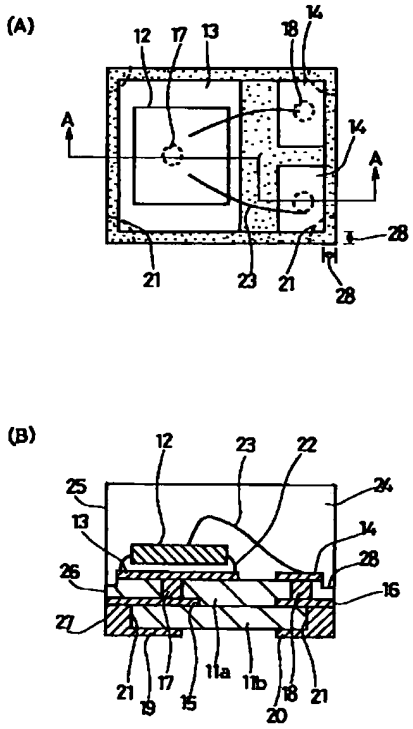
【図４】本発明の半導体装置の製造方法を説明する図である。

【図５】他の実施の形態を説明する（Ａ）平面図、（Ｂ）断面図である。

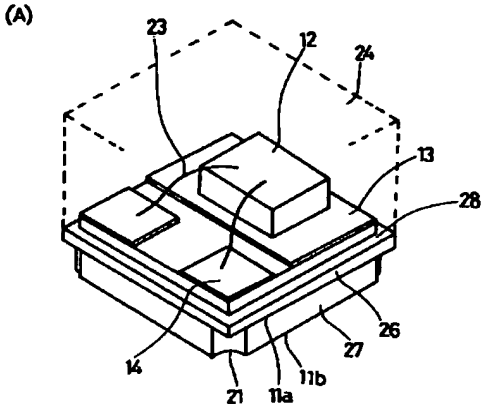
【図６】従来の半導体装置を説明する断面図である。

【図７】半導体装置を示す（Ａ）平面図、（Ｂ）断面図である。

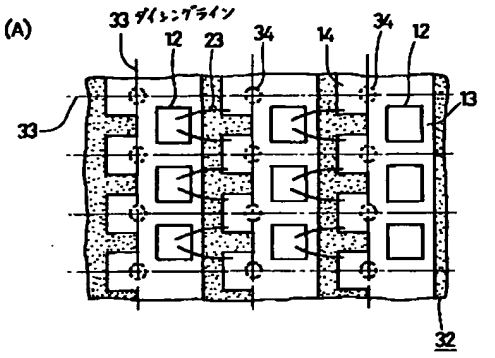
【図１】



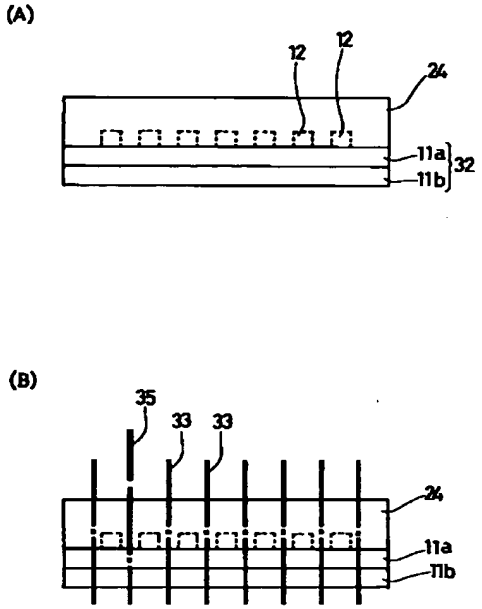
【図２】



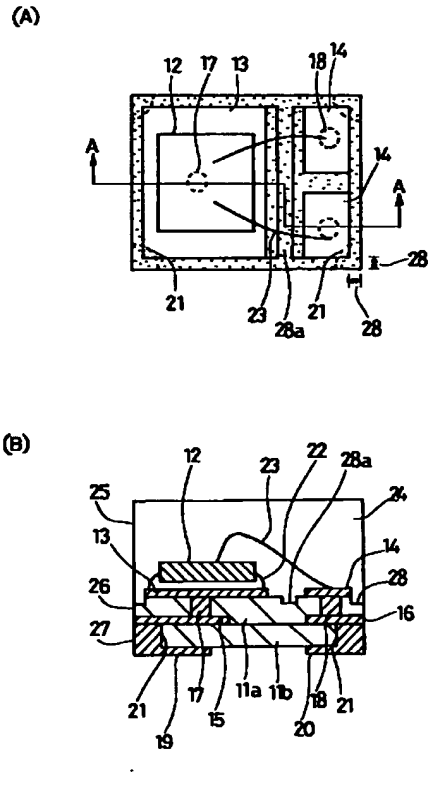
【図3】


(A)
33
ダイレクトグライン
12
23
34
14
34
12
13
33
32
(B)
28
12
23
28
14
28
13

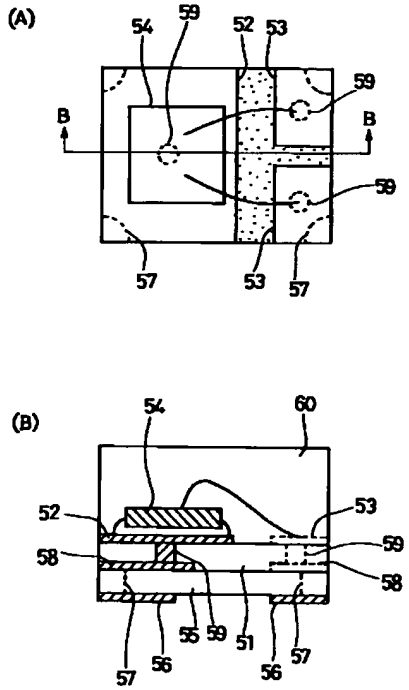
【図4】


(A)
12
12
24
11a
11b
32
(B)
35
33
33
24
11a
11b

【図5】

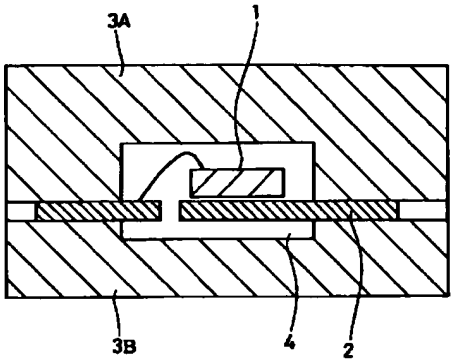

(A)
12
17
13
18
14
A
A
14
28
21
23
21
28a
28
(B)
12
23
22
28a
25
24
13
14
28
26
16
27
21
17
11a
11b
18
21
19
15
20

【図7】

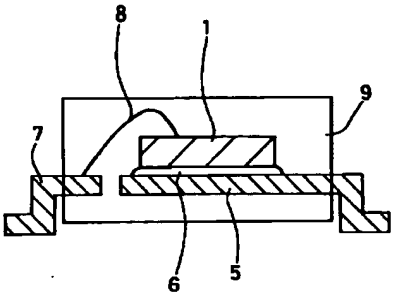

(A)
54
59
52
53
B
B
59
59
57
53
57
(B)
54
60
52
53
58
59
58
57
56
55
59
51
56
57

【図6】

(A)



(B)



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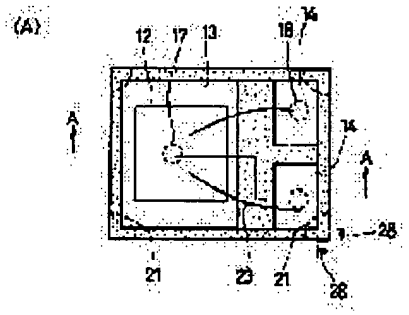
SHIBUYA TAKAO

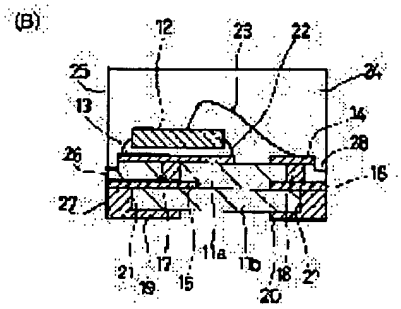
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device package, having a reduced mounting area, small in size, and freed of troubles caused by the attachment of solder at mounting.

SOLUTION: An island 13 and leads 14 are formed on the surface of a first insulating board 11a and connected electrically to outer electrodes 19 and 20 via through-holes 17 and 18 and cutouts 21 respectively. A semiconductor chip 12 is mounted on the island 13 and bonded to the leads 14 with a wire. The semiconductor chip 12 is covered with a resin layer 24, and the peripheral edge faces 26 and 27 of the first and the second insulating board, 11a and 11b, and made to be flush with the peripheral edge face 25 of the resin layer 24 by dicing so as to be a continuous same plane. Gold plating layers provided to the island 13 and the leads 14 are made to retreat from around the peripheral edge face 26.





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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About a semiconductor device, especially this invention reduces a package appearance and relates to the semiconductor device which can reduce a component-side product.
[0002]
[Description of the Prior Art] The transfer mold by metal mold and resin impregnation is used abundantly at the technique of the packaging in manufacture of a semiconductor device. The leadframe is used for this transfer mold technique, and two or more semiconductor devices by one leadframe will be manufactured to coincidence.
[0003] Drawing 6 (A) is drawing showing a transfer mold process. The closure of a semiconductor chip 1 is performed by fixing a semiconductor chip 1 to a leadframe 2 with die bond and wire bond, installing a leadframe 2 in the interior of the cavity 4 formed with the vertical metal mold 3A and 3B, and pouring in an epoxy resin into a cavity 4. A leadframe 2 is cut for every semiconductor chip after such a transfer mold process, and the semiconductor device according to individual is manufactured.
[0004] Drawing 6 (B) is drawing showing the semiconductor device manufactured by the transfer mold. Fixing mounting of the semiconductor chip 1 with which components, such as a transistor, were formed is carried out by the wax material 6, such as solder, on an island 5, the electrode pad of a semiconductor chip 1 and lead 7 are connected with a wire 8, it is covered with the resin 9 by which the circumference part of a semiconductor chip 1 agreed in the configuration of the above-mentioned cavity, and a part for the point of lead 7 is drawn by the exterior of resin 9.
[0005]
[Problem(s) to be Solved by the Invention] With the package using a conventional leadframe and a conventional transfer mold, since the lead terminal for external connection is made to project from resin, the distance to the point of a lead terminal must be taken into consideration as a component-side product, and there is a fault that the component-side product becomes large far from the dimension of resin.
[0006] Therefore, the technique of making a dimension and a component-side product almost equal by using a solder bump etc. for an external connection lead, the approach of carrying out direct die bond of the bare chip on a mounting substrate, etc. are proposed.
[0007] The applicant for this patent proposed the semiconductor device which reduced the component-side product sharply to Japanese Patent Application No. No. 262160 [nine to] by using an insulating substrate and a dicing technique to such a proposition.
[0008] This equipment forms the island section 52 and the lead section 53 in the 1st insulating substrate 51 with an electric conduction pattern with reference to drawing 7 . Carry out wire bond and the external electrode 56 is formed in the rear face of the 2nd insulating substrate 55. a semiconductor chip 54 -- die bond -- Furthermore, the notching 57 which performed electric conduction plating is formed in four corners of the 2nd insulating substrate 55, it connects with the external electrode 56, and this external electrode 56, the island section 52, and the lead section 53 are electrically connected by the middle

conductor pattern 58 and a middle through hole 59. The dimension of a package is not decided by the cavity of metal mold, but is formed by cutting by dicing with resin 60 around a semiconductor chip 54. When this is mounted, a mounting substrate is pasted with solder by using as an electrode the external electrode 56 formed in the 2nd insulating-substrate 55 rear face with the electric conduction deposit exposed to notching 57 inside. Since a lead terminal does not project, this structure can reduce a component-side product sharply. In addition, drawing 7 (B) is BB line sectional view of drawing 7 (A).
[0009] However, with this structure, it becomes resin 60 and the structure which the end face of the electric conduction pattern of the island section 52 and the lead section 53 exposed to the boundary part of the 1st insulating substrate 51. As for the gold (Au) used for an electric conduction pattern, the thing with solder for which it is smeared, solder will be adsorbed if the solder for mounting reaches the end face of said electric conduction pattern, since the sex is very high, solder trespasses upon the boundary of the 1st insulating substrate 51 and resin 60, and poor peeling is produced became clear.
[0010]
[Means for Solving the Problem] This invention is accomplished in view of each situation mentioned above, two or more semiconductor chips are carried on the substrate which stuck and formed two or more insulating substrates in the 1st, a semiconductor chip is closed in a resin layer, and the semiconductor device which can reduce the dimension and component-side product of equipment for resin and an insulating substrate sharply dicing and by cutting is offered so that a semiconductor chip may be surrounded.
[0011] It prevents and has that a conductor pattern exposes to a periphery end face the conductor pattern formed in the front face of the 1st insulating substrate by making it retreat inside from the periphery end face of the 1st insulating substrate in the 2nd, and the solder at the time of mounting prevents the accident adsorbed between a resin layer and the 1st insulating substrate.
[0012]
[Embodiment of the Invention] The gestalt of the operation of this invention to the following is explained to a detail.
[0013] The (A) top view in which drawing 1 shows the semiconductor device of this invention, (B) AA line sectional view, and drawing 2 (A) are the perspective views showing the semiconductor device of this invention. This semiconductor device is carried on the 1st and the 2nd insulating substrate 11a and 11b which consist of a ceramic whose board thickness is 150-250micro respectively, glass epoxy, etc., and the 1st insulating substrate 11, and it has the semiconductor chip 12 in which the transistor component etc. was formed.
[0014] The island section 13 and the lead section 14 are formed in the front face of 1st insulating-substrate 11a of the gold plate layer, and bipolar electrodes 15 and 16 are formed also in the rear face of 1st insulating-substrate 11a of the gold plate layer. Bipolar electrodes 15 and 16 have the pattern equivalent to the pattern of the island section 13 and the lead section 14. Through holes 17 and 18 are established in the 1st insulating-substrate 11a of the island section 13 and the lead section 14, the interior of these through holes 17 and 18 is laid underground with electrical conducting materials, such as a tungsten and Ag-Pd, and the island section 13, the bipolar electrode 15, and the lead section 14 and a bipolar electrode 16 are respectively connected electrically by this.
[0015] The external electrodes 19 and 20 are formed in the rear face of 2nd insulating-substrate 11b with the electric conduction pattern, and these external electrodes 19 and 20 have extended even near the termination of 2nd insulating-substrate 11b. The notching section 21 equivalent to the quadrant of a cylindrical shape is formed in four corners of 2nd insulating-substrate 11b, an electric conduction pattern is formed also in the inner skin of this notching section 21, and the external electrodes 19 and 20 and bipolar electrodes 15 and 16 are connected electrically. The external electrodes 19 and 20 which carry out considerable to a result and the base collector emitter of a transistor respectively are formed.
[0016] And the semiconductor chip 12 has fixed with the adhesives 22, such as a silver paste metallurgy silicon eutectic, in the island section 13, and wirebonding of the bonding pad and the lead section 14 which were formed in semiconductor chip 12 front face is carried out with the wire 23. The resin layer 24 of an epoxy system is formed on 1st insulating-substrate 11a, this is closed and the package of an

abbreviation rectangular parallelepiped is formed so that these semiconductor chips 12 and wires 23 may be covered.

[0017] An inferior surface of tongue is constituted by the resin layer 24, and, as for the appearance of a package, the rear face of 2nd insulating-substrate 11b and four side faces are respectively constituted for a top face by the periphery end faces 25, 26, and 27 of the resin layer 24, the 1st, and the 2nd insulating substrate 11a and 11b. The periphery end face 25 of the resin layer 24, and the 1st and the periphery end faces 26 and 27 of the 2nd insulating substrate 11a and 11b have constituted the same continuous horizontal plane.

[0018] And the gold plate layer of the island section 13 and the lead section 14 formed in the front face of 1st insulating-substrate 11a is not given to the periphery end face 26 of 1st insulating-substrate 11a, but the perimeter of 1st insulating-substrate 11a is covered, and only distance (30-70micro) is retreating from the edge. 30-70micro, and the about [depth 100micro] slot 28 are formed in the part which retreated for width of face so that the perimeter of a semiconductor chip 12 may be surrounded along with the periphery end face 26 of 1st insulating-substrate 11a.

[0019] Drawing 2 (B) is the sectional view showing the condition of having mounted this equipment. In the printed circuit 30 for network formation formed on the mounting substrate 29, location ****** of the external electrodes 19 and 20 of equipment is carried out, and equipment fixes with solder. With surface tension, solder rises at the edge and forms the solder fillet 31.

[0020] If it is the semiconductor device of this invention, since the inside of the notching section 21 is covered with electric conduction patterns, such as a gold plate layer, the solder fillet 31 can be heaped up greatly. Since these gold plate layers are not exposed to the boundary of the resin layer 24 and 1st insulating-substrate 11a by having retreated the island section 13 and the lead section 14 at this time, the solder of the solder fillet 31 is not absorbed. Therefore, the accident on which the resin layer 24 exfoliates is avoidable. Moreover, since the faying surface product of 1st insulating-substrate 11a and the resin layer 24 increases by having formed the slot 28, both bond strength can be increased.

[0021] The semiconductor device explained above can be obtained by the following approaches.

[0022] 1st process: -- drawing 3 (A) -- the large-sized substrate 32 which is equivalent to a part for equipment plurality first of all 3 ** is prepared. This substrate 32 sticks the 1st and the 2nd insulating substrate 11a and 11b. The pattern corresponding to an island 13 and the lead section 14 is drawn by the front face of 1st insulating-substrate 11a by the ctenidium-like continuation pattern by the gold plate layer. The gold plate layer corresponding to the external electrodes 19 and 20 is formed by the same continuation pattern also as the rear face of 2nd insulating-substrate 11b. The through holes 17 and 18 for taking the external electrodes 19 and 20 and electrical installation are established in the 1st insulating-substrate 11a of an island 13 and the lead section 14. In this phase, the island section 13 and the lead section 14 are continuous patterns which have not been separated.

[0023] In this drawing, the field surrounded with the dicing line 33 will be behind started as one semiconductor device. And the through hole 34 equivalent to notching 21 is established in the 2nd insulating-substrate 11b of the part where the dicing line 33 crosses.

[0024] it is alike, the substrate 32 of this condition is received, die bond of many semiconductor chips 12 is carried out, and the bonding pad and the lead section 14 which were formed on the chip are connected by the bonding wire 23.

[0025] The 2nd process: Drawing 3 (B)

By using the dicing line 33 as a center line, width of face 50-80micro and the slot 28 with a depth of about 100micro are formed so that this may be met. A slot 28 is formed by carrying out the dicing of the 1st insulating-substrate 11a front face with a gold plate layer using a dicing blade. Thereby, while forming a slot 28, the island section 13 and the lead section 14 can be retreated from the dicing line 33.

[0026] The 3rd process: Drawing 4 (A)

The resin layer 24 is formed by technique, such as potting, on 1st insulating-substrate 11a. The resin layer 24 does not cover a semiconductor chip 12 according to an individual, and covers two or more semiconductor chips 12 with continuous resin collectively. For example, when 50 semiconductor chips 12 are carried in one substrate 32, all 50 chips are covered collectively.

[0027] The 4th process: Drawing 4 (B)
With the dicing blade 35, the resin layer 24, the 1st, and the 2nd insulating substrate 11a and 11b are cut to coincidence along the dicing line 33, and it separates into each semiconductor device. At this process, the dicing blade with board thickness narrower than the width of face of a slot 28 is used, it left the slot 28 to the periphery end face 26 of 1st insulating-substrate 11a by this, and the structure which the gold plate layer of the island section 13 and the lead section 14 does not expose to the periphery end face 25 of the resin layer 24 has been acquired. Moreover, the through hole 34 established in a part for the intersection of the dicing line 33 is quadrisected by dicing, and forms the notching section 21. Furthermore, those cutting planes (periphery end faces 25, 26, and 27) consist of same flat surfaces by constituting four side faces of a package by dicing.
[0028] The semiconductor device manufactured by the above approach has the following merits.
[0029] The resin ingredient made useless compared with the case where packaging is carried out separately since packaging of many components is collectively carried out by resin can be lessened, and it is **. It leads to reduction of the cost of materials.
[0030] The alignment accuracy of dicing equipment has about plus minus 10micro and a high precision to the alignment precision of mold metal mold and a leadframe being about plus minus 50micro. Therefore, if a resin appearance is formed by dicing, thickness from the island section 13 to the cutting plane of resin 21 can be made thin, the small package of a dimension can be obtained more, and also if it compares with the same dimension, the area of the island section 13 is increased and the semiconductor chip 12 which can be carried can be enlarged.
[0031] In addition, in case it replaces with a means to form a slot 28 by dicing and the pattern of the island section 13 and the lead section 14 is formed, structure with the same said of forming by the pattern beforehand retreated from the dicing line 26 can be acquired.
[0032] Furthermore, as shown in drawing 5 , it is also possible by forming slot 28a in formation and the coincidence target of a slot 28 also at the null part between the island section 13 and the lead section 14 to improve adhesion reinforcement with resin further.
[0033] With this operation gestalt, although the transistor was formed in the semiconductor chip 12, if it is the device of a vertical mold or a horizontal type with comparatively little calorific value, even if it is the semiconductor chip in which devices, such as not only this but power metal-oxide semiconductor field effect transistor, IGBT, HBT, etc., were formed, it is not necessary to explain that application is possible for this invention.
[0034]
[Effect of the Invention] As explained above, according to this invention, it has the advantage which can offer the package structure which can be further miniaturized rather than the semiconductor device using a leadframe. Since it is the structure where a lead terminal does not project, at this time, the occupancy area when mounting is reduced and high density assembly can be realized.
[0035] Furthermore, it is made to the structure where the solder fillet 31 rises easily by the notching section 21. Since it considered as the configuration which a gold plate layer does not expose to the boundary part of 1st insulating-substrate 11a and the resin layer 24 at this time, the solder at the time of mounting can avoid contact and the accident on which it absorbs and the resin layer 24 exfoliates into a boundary part.
[0036] In addition, the adhesion force of 1st insulating-substrate 11a and the resin layer 24 can be increased by forming a slot 28 in the periphery part of 1st insulating-substrate 11a, and also retreat of a gold plate layer and formation of a slot 28 can be carried out instantaneous by forming a slot 28 by dicing. It can ******.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] About a semiconductor device, especially this invention reduces a package appearance and relates to the semiconductor device which can reduce a component-side product.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] The transfer mold by metal mold and resin impregnation is used abundantly at the technique of the packaging in manufacture of a semiconductor device. The leadframe is used for this transfer mold technique, and two or more semiconductor devices by one leadframe will be manufactured to coincidence.
[0003] Drawing 6 (A) is drawing showing a transfer mold process. The closure of a semiconductor chip 1 is performed by fixing a semiconductor chip 1 to a leadframe 2 with die bond and wire bond, installing a leadframe 2 in the interior of the cavity 4 formed with the vertical metal mold 3A and 3B, and pouring in an epoxy resin into a cavity 4. A leadframe 2 is cut for every semiconductor chip after such a transfer mold process, and the semiconductor device according to individual is manufactured.
[0004] Drawing 6 (B) is drawing showing the semiconductor device manufactured by the transfer mold. Fixing mounting of the semiconductor chip 1 with which components, such as a transistor, were formed is carried out by the wax material 6, such as solder, on an island 5, the electrode pad of a semiconductor chip 1 and lead 7 are connected with a wire 8, it is covered with the resin 9 by which the circumference part of a semiconductor chip 1 agreed in the configuration of the above-mentioned cavity, and a part for the point of lead 7 is drawn by the exterior of resin 9.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, it has the advantage which can offer the package structure which can be further miniaturized rather than the semiconductor device using a leadframe. Since it is the structure where a lead terminal does not project, at this time, the occupancy area when mounting is reduced and high density assembly can be realized.
[0035] Furthermore, it is made to the structure where the solder fillet 31 rises easily by the notching section 21. Since it considered as the configuration which a gold plate layer does not expose to the boundary part of 1st insulating-substrate 11a and the resin layer 24 at this time, the solder at the time of mounting can avoid contact and the accident on which it absorbs and the resin layer 24 exfoliates into a boundary part.
[0036] In addition, the adhesion force of 1st insulating-substrate 11a and the resin layer 24 can be increased by forming a slot 28 in the periphery part of 1st insulating-substrate 11a, and also retreat of a gold plate layer and formation of a slot 28 can be carried out instantaneous by forming a slot 28 by dicing. It can ******.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] With the package using a conventional leadframe and a conventional transfer mold, since the lead terminal for external connection is made to project from resin, the distance to the point of a lead terminal must be taken into consideration as a component-side product, and there is a fault that the component-side product becomes large far from the dimension of resin.
[0006] Therefore, the technique of making a dimension and a component-side product almost equal by using a solder bump etc. for an external connection lead, the approach of carrying out direct die bond of the bare chip on a mounting substrate, etc. are proposed.
[0007] The applicant for this patent proposed the semiconductor device which reduced the component-side product sharply to Japanese Patent Application No. No. 262160 [nine to] by using an insulating substrate and a dicing technique to such a proposition.
[0008] This equipment forms the island section 52 and the lead section 53 in the 1st insulating substrate 51 with an electric conduction pattern with reference to drawing 7 . Carry out wire bond and the external electrode 56 is formed in the rear face of the 2nd insulating substrate 55. a semiconductor chip 54 -- die bond -- Furthermore, the notching 57 which performed electric conduction plating is formed in four corners of the 2nd insulating substrate 55, it connects with the external electrode 56, and this external electrode 56, the island section 52, and the lead section 53 are electrically connected by the middle conductor pattern 58 and a middle through hole 59. The dimension of a package is not decided by the cavity of metal mold, but is formed by cutting by dicing with resin 60 around a semiconductor chip 54. When this is mounted, a mounting substrate is pasted with solder by using as an electrode the external electrode 56 formed in the 2nd insulating-substrate 55 rear face with the electric conduction deposit exposed to notching 57 inside. Since a lead terminal does not project, this structure can reduce a component-side product sharply. In addition, drawing 7 (B) is BB line sectional view of drawing 7 (A).
[0009] However, with this structure, it becomes resin 60 and the structure which the end face of the electric conduction pattern of the island section 52 and the lead section 53 exposed to the boundary part of the 1st insulating substrate 51. As for the gold (Au) used for an electric conduction pattern, the thing with solder for which it is smeared, solder will be adsorbed if the solder for mounting reaches the end face of said electric conduction pattern, since the sex is very high, solder trespasses upon the boundary of the 1st insulating substrate 51 and resin 60, and poor peeling is produced became clear.

[Translation done.]

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MEANS

[Means for Solving the Problem] This invention is accomplished in view of each situation mentioned above, two or more semiconductor chips are carried on the substrate which stuck and formed two or more insulating substrates in the 1st, a semiconductor chip is closed in a resin layer, and the semiconductor device which can reduce the dimension and component-side product of equipment for resin and an insulating substrate sharply dicing and by cutting is offered so that a semiconductor chip may be surrounded.
[0011] It prevents and has that a conductor pattern exposes to a periphery end face the conductor pattern formed in the front face of the 1st insulating substrate by making it retreat inside from the periphery end face of the 1st insulating substrate in the 2nd, and the solder at the time of mounting prevents the accident adsorbed between a resin layer and the 1st insulating substrate.
[0012]
[Embodiment of the Invention] The gestalt of the operation of this invention to the following is explained to a detail.
[0013] The (A) top view in which drawing 1 shows the semiconductor device of this invention, (B) AA line sectional view, and drawing 2 (A) are the perspective views showing the semiconductor device of this invention. This semiconductor device is carried on the 1st and the 2nd insulating substrate 11a and 11b which consist of a ceramic whose board thickness is 150-250micro respectively, glass epoxy, etc., and the 1st insulating substrate 11, and it has the semiconductor chip 12 in which the transistor component etc. was formed.
[0014] The island section 13 and the lead section 14 are formed in the front face of 1st insulating-substrate 11a of the gold plate layer, and bipolar electrodes 15 and 16 are formed also in the rear face of 1st insulating-substrate 11a of the gold plate layer. Bipolar electrodes 15 and 16 have the pattern equivalent to the pattern of the island section 13 and the lead section 14. Through holes 17 and 18 are established in the 1st insulating-substrate 11a of the island section 13 and the lead section 14, the interior of these through holes 17 and 18 is laid underground with electrical conducting materials, such as a tungsten and Ag-Pd, and the island section 13, the bipolar electrode 15, and the lead section 14 and a bipolar electrode 16 are respectively connected electrically by this.
[0015] The external electrodes 19 and 20 are formed in the rear face of 2nd insulating-substrate 11b with the electric conduction pattern, and these external electrodes 19 and 20 have extended even near the termination of 2nd insulating-substrate 11b. The notching section 21 equivalent to the quadrant of a cylindrical shape is formed in four corners of 2nd insulating-substrate 11b, an electric conduction pattern is formed also in the inner skin of this notching section 21, and the external electrodes 19 and 20 and bipolar electrodes 15 and 16 are connected electrically. The external electrodes 19 and 20 which carry out considerable to a result and the base collector emitter of a transistor respectively are formed.
[0016] And the semiconductor chip 12 has fixed with the adhesives 22, such as a silver paste metallurgy silicon eutectic, in the island section 13, and wirebonding of the bonding pad and the lead section 14 which were formed in semiconductor chip 12 front face is carried out with the wire 23. The resin layer 24 of an epoxy system is formed on 1st insulating-substrate 11a, this is closed and the package of an

abbreviation rectangular parallelepiped is formed so that these semiconductor chips 12 and wires 23 may be covered.

[0017] An inferior surface of tongue is constituted by the resin layer 24, and, as for the appearance of a package, the rear face of 2nd insulating-substrate 11b and four side faces are respectively constituted for a top face by the periphery end faces 25, 26, and 27 of the resin layer 24, the 1st, and the 2nd insulating substrate 11a and 11b. The periphery end face 25 of the resin layer 24, and the 1st and the periphery end faces 26 and 27 of the 2nd insulating substrate 11a and 11b have constituted the same continuous horizontal plane.

[0018] And the gold plate layer of the island section 13 and the lead section 14 formed in the front face of 1st insulating-substrate 11a is not given to the periphery end face 26 of 1st insulating-substrate 11a, but the perimeter of 1st insulating-substrate 11a is covered, and only distance (30-70micro) is retreating from the edge. 30-70micro, and the about [depth 100micro] slot 28 are formed in the part which retreated for width of face so that the perimeter of a semiconductor chip 12 may be surrounded along with the periphery end face 26 of 1st insulating-substrate 11a.

[0019] Drawing 2 (B) is the sectional view showing the condition of having mounted this equipment. In the printed circuit 30 for network formation formed on the mounting substrate 29, location ****** of the external electrodes 19 and 20 of equipment is carried out, and equipment fixes with solder. With surface tension, solder rises at the edge and forms the solder fillet 31.

[0020] If it is the semiconductor device of this invention, since the inside of the notching section 21 is covered with electric conduction patterns, such as a gold plate layer, the solder fillet 31 can be heaped up greatly. Since these gold plate layers are not exposed to the boundary of the resin layer 24 and 1st insulating-substrate 11a by having retreated the island section 13 and the lead section 14 at this time, the solder of the solder fillet 31 is not absorbed. Therefore, the accident on which the resin layer 24 exfoliates is avoidable. Moreover, since the faying surface product of 1st insulating-substrate 11a and the resin layer 24 increases by having formed the slot 28, both bond strength can be increased.

[0021] The semiconductor device explained above can be obtained by the following approaches.

[0022] 1st process: -- drawing 3 (A) -- the large-sized substrate 32 which is equivalent to a part for equipment plurality first of all 3 ** is prepared. This substrate 32 sticks the 1st and the 2nd insulating substrate 11a and 11b. The pattern corresponding to an island 13 and the lead section 14 is drawn by the front face of 1st insulating-substrate 11a by the ctenidium-like continuation pattern by the gold plate layer. The gold plate layer corresponding to the external electrodes 19 and 20 is formed by the same continuation pattern also as the rear face of 2nd insulating-substrate 11b. The through holes 17 and 18 for taking the external electrodes 19 and 20 and electrical installation are established in the 1st insulating-substrate 11a of an island 13 and the lead section 14. In this phase, the island section 13 and the lead section 14 are continuous patterns which have not been separated.

[0023] In this drawing, the field surrounded with the dicing line 33 will be behind started as one semiconductor device. And the through hole 34 equivalent to notching 21 is established in the 2nd insulating-substrate 11b of the part where the dicing line 33 crosses.

[0024] it is alike, the substrate 32 of this condition is received, die bond of many semiconductor chips 12 is carried out, and the bonding pad and the lead section 14 which were formed on the chip are connected by the bonding wire 23.

[0025] The 2nd process: Drawing 3 (B)

By using the dicing line 33 as a center line, width of face 50-80micro and the slot 28 with a depth of about 100micro are formed so that this may be met. A slot 28 is formed by carrying out the dicing of the 1st insulating-substrate 11a front face with a gold plate layer using a dicing blade. Thereby, while forming a slot 28, the island section 13 and the lead section 14 can be retreated from the dicing line 33.

[0026] The 3rd process: Drawing 4 (A)

The resin layer 24 is formed by technique, such as potting, on 1st insulating-substrate 11a. The resin layer 24 does not cover a semiconductor chip 12 according to an individual, and covers two or more semiconductor chips 12 with continuous resin collectively. For example, when 50 semiconductor chips 12 are carried in one substrate 32, all 50 chips are covered collectively.

[0027] The 4th process: Drawing 4 (B)
With the dicing blade 35, the resin layer 24, the 1st, and the 2nd insulating substrate 11a and 11b are cut to coincidence along the dicing line 33, and it separates into each semiconductor device. At this process, the dicing blade with board thickness narrower than the width of face of a slot 28 is used, it left the slot 28 to the periphery end face 26 of 1st insulating-substrate 11a by this, and the structure which the gold plate layer of the island section 13 and the lead section 14 does not expose to the periphery end face 25 of the resin layer 24 has been acquired. Moreover, the through hole 34 established in a part for the intersection of the dicing line 33 is quadrisected by dicing, and forms the notching section 21. Furthermore, those cutting planes (periphery end faces 25, 26, and 27) consist of same flat surfaces by constituting four side faces of a package by dicing.
[0028] The semiconductor device manufactured by the above approach has the following merits.
[0029] The resin ingredient made useless compared with the case where packaging is carried out separately since packaging of many components is collectively carried out by resin can be lessened, and it is **. It leads to reduction of the cost of materials.
[0030] The alignment accuracy of dicing equipment has about plus minus 10micro and a high precision to the alignment precision of mold metal mold and a leadframe being about plus minus 50micro. Therefore, if a resin appearance is formed by dicing, thickness from the island section 13 to the cutting plane of resin 21 can be made thin, the small package of a dimension can be obtained more, and also if it compares with the same dimension, the area of the island section 13 is increased and the semiconductor chip 12 which can be carried can be enlarged.
[0031] In addition, in case it replaces with a means to form a slot 28 by dicing and the pattern of the island section 13 and the lead section 14 is formed, structure with the same said of forming by the pattern beforehand retreated from the dicing line 26 can be acquired.
[0032] Furthermore, as shown in drawing 5 , it is also possible by forming slot 28a in formation and the coincidence target of a slot 28 also at the null part between the island section 13 and the lead section 14 to improve adhesion reinforcement with resin further.
[0033] With this operation gestalt, although the transistor was formed in the semiconductor chip 12, if it is the device of a vertical mold or a horizontal type with comparatively little calorific value, even if it is the semiconductor chip in which devices, such as not only this but power metal-oxide semiconductor field effect transistor, IGBT, HBT, etc., were formed, it is not necessary to explain that application is possible for this invention.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the (A) top view and the (B) sectional view showing the semiconductor device of this invention.
[Drawing 2] It is the (A) perspective view and the (B) sectional view showing the semiconductor device of this invention.
[Drawing 3] It is drawing explaining the manufacture approach of the semiconductor device of this invention.
[Drawing 4] It is drawing explaining the manufacture approach of the semiconductor device of this invention.
[Drawing 5] It is the (A) top view and the (B) sectional view explaining the gestalt of other operations.
[Drawing 6] It is a sectional view explaining the conventional semiconductor device.
[Drawing 7] It is the (A) top view and the (B) sectional view showing a semiconductor device.

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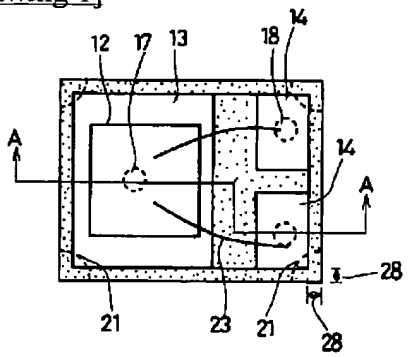
DRAWINGS

[Drawing 1]

(A)



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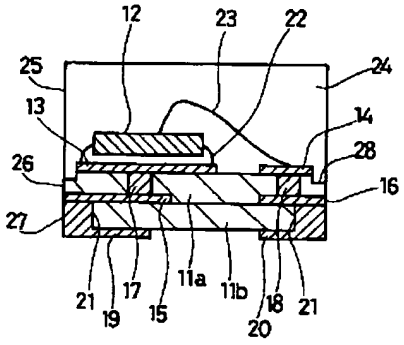
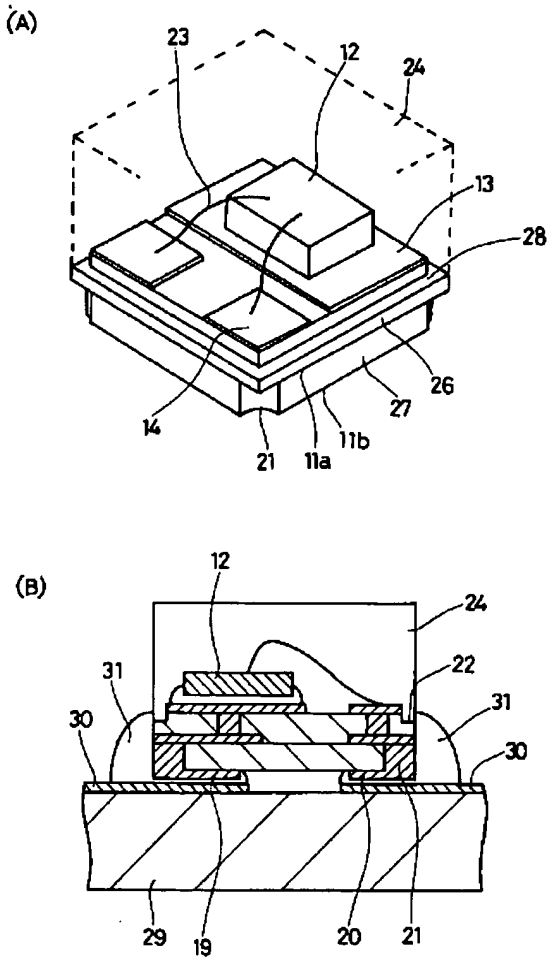
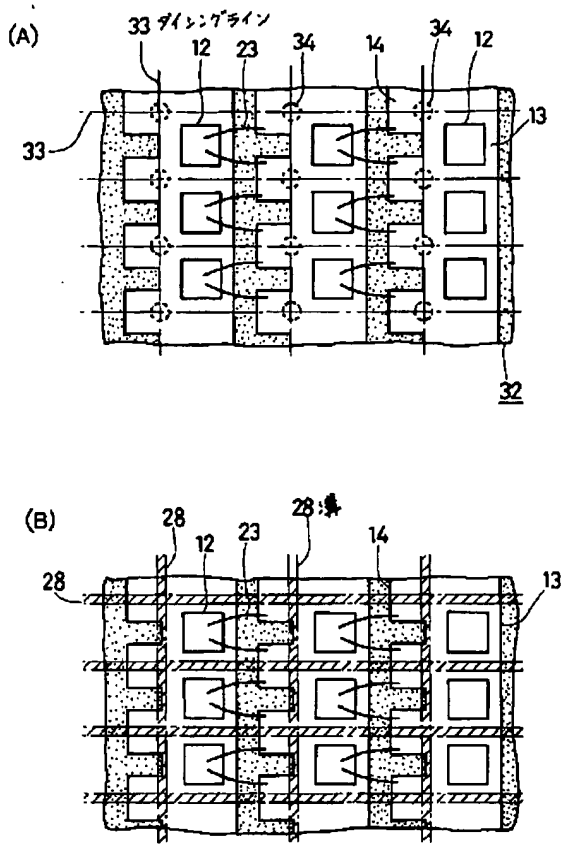


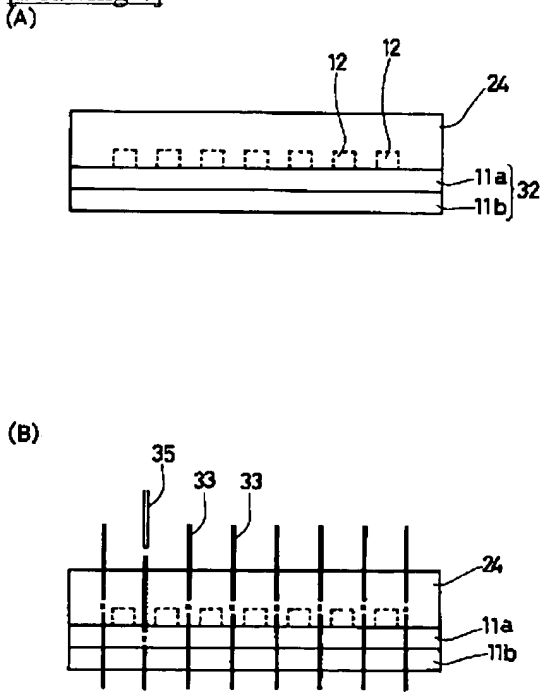
[Drawing 2]



[Drawing 3]

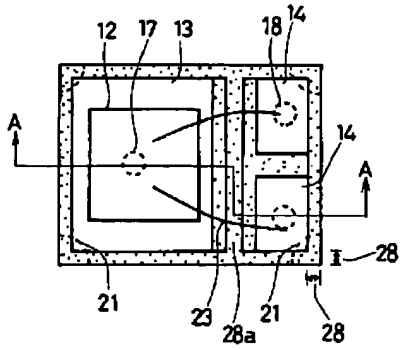


[Drawing 4]



[Drawing 5]

(A)



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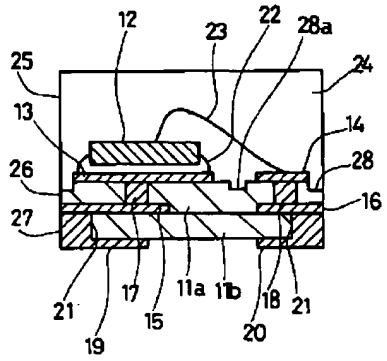
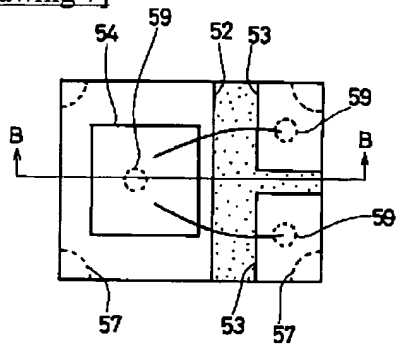


[Drawing 7]

(A)



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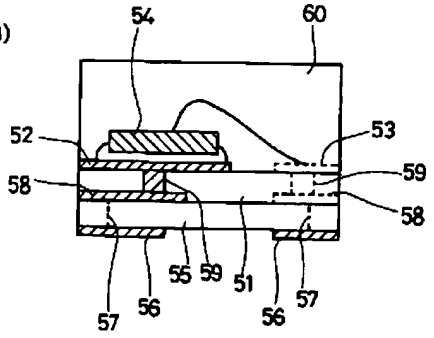
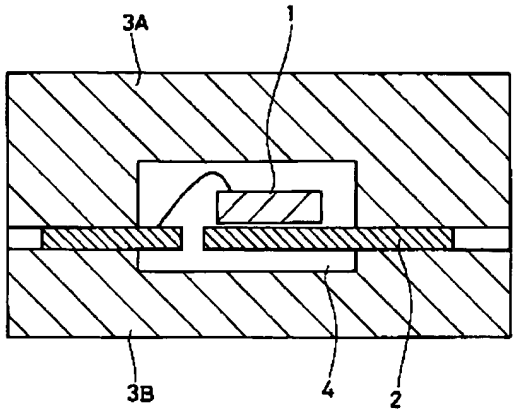


[Drawing 6]

(A)



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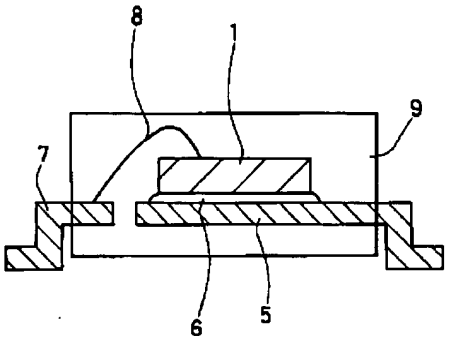

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CLAIMS

[Claim(s)]
[Claim 1] The 1st and the 2nd insulating substrate which stick and form a support substrate, and the island section formed in the front face of said 1st insulating substrate with the conductor pattern and the lead section, A means to connect electrically the semiconductor chip carried in said island section, and the electrode and said lead section of said semiconductor chip, The resin layer which is prepared on said 1st insulating substrate and covers said semiconductor chip and said island section, and said lead section, The bipolar electrode prepared between said 1st insulating substrate and 2nd insulating substrate, and the external electrode which was formed in the rear-face side of said 2nd insulating substrate, and was electrically connected with said island section or the lead section through said bipolar electrode, The notching section by which it was prepared in the corner of said 2nd insulating substrate, and the electric conduction pattern which follows said external electrode was prepared in the front face, Said the 1st and periphery end face of the 2nd insulating substrate, and the periphery end face of said resin layer are provided. Said the 1st, periphery end face of the 2nd insulating substrate, and periphery end face of said resin layer are mostly in agreement. The semiconductor device characterized by having located the conductor pattern of said island section and said lead section inside said periphery end face, and said the 1st material and said resin layer of an insulating substrate having stuck near [said] a periphery end face.
[Claim 2] The semiconductor device according to claim 1 characterized by consisting of cutting planes from which said periphery end face cut said resin layer, said 1st [the], and 2nd insulating substrate to coincidence.
[Claim 3] The semiconductor device according to claim 1 characterized by preparing a slot near the periphery end face of said 1st insulating substrate.
[Claim 4] The 1st insulating substrate in which the conductor pattern for forming two or more semiconductor devices in the front face was formed, The process which sticks so that the 2nd insulating substrate in which the external electrode for external connection was formed may be electrically connected in said conductor pattern and said external electrode, and constitutes a large-sized substrate, The process which retreats said conductor pattern from the edge of said 1st insulating substrate, The process which covers the upper part of said 1st insulating substrate with a resin layer, and around said semiconductor chip so that the process which fixes a semiconductor chip to said conductor pattern, and said semiconductor chip may be covered The manufacture approach of the semiconductor device characterized by providing the process which cuts said resin layer, said 1st [the], and 2nd insulating substrate, and separates said semiconductor device separately.
[Claim 5] The manufacture approach of the semiconductor device according to claim 4 characterized by retreating said conductor pattern from the package periphery presumptive region by carrying out the dicing of the front face of said 1st insulating substrate with said conductor pattern.

[Translation done.]